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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/809,147	03/14/2001	Toshiaki Kato	SQR-P1	5354

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LEIGHTON K. CHONG
OSTRAGER CHONG & FLAHERTY (HAWAII)
841 BISHOP STREET, SUITE 1200
HONOLULU, HI 96813

EXAMINER

ALI, SYED J

ART UNIT	PAPER NUMBER
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2127

DATE MAILED: 06/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/809,147

Applicant(s)

KATO, TOSHIAKI

Examiner

Syed J Ali

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 March 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 March 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>5/24/01</u> . | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

1. Claims 1-20 are pending in this application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. **Claims 1-3, 7-14, and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki (USPN 5,673,380) in view of Keller et al. (USPN 5,010,482) (hereinafter Keller).**

4. As per claim 1, Suzuki teaches the invention as claimed, including a parallel processing method for performing processing tasks in parallel on a plurality of processors comprising:

(a) breaking down a processing task into a plurality of self-contained task objects (col. 4 line 58 - col. 5 line 47), wherein each task object is defined with a computational task and at least one "data-waiting" slot for receipt of data requested from another task object to which the processing task passes a message for the requested data (col. 7 line 64 - col. 8 line 26), and wherein once all the "data-waiting" slots of a task object are filled by the respective return message(s), the task object can perform its defined computational task without waiting for any other input (col. 7 line 64 - col. 8 line 26);

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(b) scheduling the defined task objects to be processed by distributing them across the plurality of processors, by:

(i) placing a task object with an unfilled "data-waiting" slot in a "waiting" state in which it is not assigned to any processor (col. 5 line 61 - col. 6 line 14; col. 7 line 64 - col. 8 line 26);

(ii) changing the status of a task object to an "active" state when all of its defined "data-waiting" slots have been filled (col. 5 line 60 - col. 6 line 14); and

(iii) changing the status of the task object to a "dead" state when the computational task to be performed for the task object by the assigned processor has been completed (col. 8 lines 45-56).

5. Keller teaches the invention as claimed, including wherein the task is assigned to a next available processor in an "unoccupied" state when its data is available, then placing that processor's status in an "occupied" state (col. 3 lines 15-23; col. 7 lines 8-29; col. 15 line 51 - col. 16 line 7); and

changing the processor's status to an "unoccupied" state to be assigned to a next "active" task object when the task is complete (col. 3 lines 15-23; col. 7 lines 8-29; col. 15 line 51 - col. 16 line 7).

6. It would have been obvious to one of ordinary skill in the art to combine Suzuki and Keller since the act of parallel processing requires a system to make efficient use of resources. Assigning a task that is waiting on data to a processor is highly inefficient since the amount of time spent waiting for data may be high, causing a system bottleneck. Additionally, tracking the

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status of the system's processors prevents further bottlenecking by ensuring that a processor is capable of satisfying a request before assigning it a task.

7. As per claim 2, Suzuki teaches the invention as claimed, including a parallel processing method according to Claim 1, wherein a master task grouping is defined by a plurality of task spaces each of which contains multiple task objects and does not require message passing from an external source in order to complete computation for the respective task space (col. 2 lines 22-58).

8. As per claim 3, Keller teaches the invention as claimed, including a parallel processing method according to Claim 2, wherein all task objects of the task spaces which are in an "active" state are placed in a processing queue and each is assigned in turn to a next available "unoccupied" processor (col. 3 lines 15-23; col. 7 lines 8-29; col. 15 line 51 - col. 16 line 7).

9. As per claim 7, Suzuki teaches the invention as claimed, including a parallel processing method according to Claim 1, wherein the processing task includes shading an image frame of a scene in computer graphics rendering (col. 5 lines 8-47).

10. As per claim 8, Suzuki teaches the invention as claimed, including a parallel processing method according to Claim 7, wherein the shading task includes a master task grouping of shading task spaces each of which performs shading of a pixel in the image frame (col. 5 lines 48-60).

11. As per claim 9, Suzuki teaches the invention as claimed, including a parallel processing method according to Claim 8, wherein each shading task space includes a plurality of “pixel shading” task objects for performing shading of the pixel based upon ray shooting from light sources in the scene, and a “compositing” task object for compositing the shading results for the pixel (col. 5 lines 8-60).

12. As per claim 10, Suzuki teaches the invention as claimed, including a parallel processing method according to Claim 9, wherein each shading task object has at least one “data-waiting” slot for return of data characterizing light emitted from a respective light source in the scene (col. 5 lines 8-47).

13. As per claim 11, Suzuki teaches the invention as claimed, including a parallel processing method according to Claim 9, wherein the rendering task includes a function for receiving scene data for a “world map” of the scene, a function for defining the scene objects in each frame of the scene, a function for defining the pixels of an object in the scene intersected by an eye ray of a viewer of the scene, and a function for tiling together the shading results returned by each of the master shading task groupings for respective objects in the image frame (col. 5 lines 8-47).

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14. As per claims 12-14 and 19-20, Suzuki teaches the invention as claimed, including a software programming method for performing processing tasks in parallel on a plurality of processors comprising the method steps of claims 1-3 and 7-8, respectively (col. 4 line 42 - col. 5 line 47).

15. As per claim 18, Suzuki teaches the invention as claimed, including a software programming method according to Claim 12, further comprising storing templates for different types of task engines, spaces, and objects in a library and utilizing the templates to generate software programming for a desired processing task (col. 5 lines 8-47).

16. **Claims 4-6 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki in view of Keller as applied to claims 3 and 14 above, respectively, and further in view of Brobst et al. (USPN 6,125,382) (hereinafter Brobst).**

17. As per claim 4, Brobst teaches the invention as claimed, including the following limitations not shown by the modified Suzuki:

a parallel processing method according to Claim 3, wherein a master engine for the master task grouping maintains threads which track the processing of task objects in each of the task spaces (col. 5 lines 40-56).

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18. It would have been obvious to one of ordinary skill in the art to combine the modified Suzuki and Brobst since threads of control allow a process to be encapsulated within special data structures that are more easily scheduled. Specifically, within a parallel processing system, threads of control may allow multiple tasks to be concurrently executing on the same processor. Many thread scheduling algorithms are well known that are capable of handling data dependencies such that threads do not become blocked or starved. The use of threads allows the system to maximize the available processing resources.

19. As per claim 5, Brobst teaches the invention as claimed, including a parallel processing method according to Claim 4, wherein the master engine for the master task grouping maintains an internal space address assigned to each respective task object (col. 5 lines 40-56).

20. As per claim 6, Brobst teaches the invention as claimed, including a parallel processing method according to Claim 5, wherein a task object in one master task grouping can exchange data with a task object in another master task grouping by providing its internal space address indexed to its master task grouping (col. 1 lines 36-46; col. 5 lines 40-56;).

21. As per claims 15-17, Suzuki teaches the invention as claimed, including a software programming method for performing processing tasks in parallel on a plurality of processors comprising the method steps of claims 4-6, respectively (col. 4 line 42 - col. 5 line 47).

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Conclusion

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kurtzberg et al. (USPN 5,710,700) and Robertazzi et al. (USPN 6,370,560) teach a scheduling algorithm that uses a processor's availability to determine task placement.

Pfeffer et al. (USPN 5,761,734) teaches a tokenized system of processing that will not schedule a process to execute until all the data required for completion of the process is available.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Syed J Ali whose telephone number is (703) 305-8106. The examiner can normally be reached on Mon-Fri 8-5:30, 2nd Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai T An can be reached on (703) 305-9678. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Syed Ali
May 17, 2001



MENG-AI T. AN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100